REMARKS

The Examiner rejected claims 1-4, 6, 11-15 and 19 under 35 U.S.C. § 102(e) as allegedly being anticipated by Lindsay *et al.* (U.S. Pat. 6,677,778).

The Examiner rejected claims 5 and 20 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lindsay *et al.*

The Examiner rejected claims 7-10 and 16-18 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lindsay *et al.* in view of Martin *et al.* (U.S. Pat. 6,639,423).

Applicants respectfully traverse the § 102 and § 103 rejections with the following arguments.

35 U.S.C. § 102(e)

The Examiner rejected claims 1-4, 6, 11-15 and 19 under 35 U.S.C. § 102(e) as allegedly being anticipated by Lindsay *et al.* (U.S. Pat. 6,677,778).

Claims 1 and 11

Applicants respectfully contend that Lindsay does not anticipate claims 1 and 11 as amended because Lindsay does not teach each and every feature of claims 1 and 11.

First example

As a first example, Applicants respectfully contend that Lindsay does not teach the feature of "a transmitter, receiver, and transmission line formed within the semiconductor device...wherein each of said **transmitter** and said **receiver is external** to said first core and said second core " (emphasis added).

The Examiner alleges that "Lindsey et al. teaches all claimed features in Fig. 1, a semiconductor device comprising: a transmitter **(within 11)**, receiver **(within 12)**, and transmission line (130) formed within the semiconductor device, wherein the transmitter, receiver, and transmission line are adapted to control data transfer (signal) between a **first core (11)** and a **second core (12)** within the semiconductor device, wherein the transmitter is adapted to send a signal (data) over the transmission line (130) to the receiver adapted to receive the signal, *wherein* the receiver is further adapted to create (131) an impedance mismatch (reflection) to indicate that the second core is unable to transfer the data, and wherein the transmitter is adapted to detect the impedance mismatch (the reflection) "

In response, Applicants respectfully contend that Lindsey does not teach that a semiconductor device comprises a **transmitter** and **receiver** that is **external** to a first core and a second core as taught by Applicant's Claims 1 and 11. In contrast, Lindsey teaches in FIG. 1, receiving circuitry located **within** a semiconductor chip 11 and receiving circuitry located **within** a semiconductor chip 10. The Examiner alleges that "Lindsey et al. teaches..a transmitter **(within 11)**, receiver **(within 12)** ". Therefore, Applicants contend that Lindsey does not teach a transmitter and receiver that is **external** to a first core and a second core as taught by Applicant's Claims 1 and 11.

Second example

As a second example, Applicants respectfully contend that Lindsey does not teach the feature of "a transmitter, receiver, and transmission line formed within the semiconductor device...wherein said transmitter comprises a line driver, wherein said receiver comprises a line receiver, wherein said transmission line electrically connects an **output** of said line **driver to** an **input** of said line receiver ".

The Examiner alleges that "Lindsey et al. teaches all claimed features in Fig. 1, a semiconductor device comprising: a transmitter (within 11), receiver (within 12), and transmission line (130) formed within the semiconductor device, wherein the transmitter, receiver, and transmission line are adapted to control data transfer (signal) between a first core (11) and a second core (12) within the semiconductor device, wherein the transmitter is adapted to send a signal (data) over the transmission line (130) to the receiver adapted to receive the signal, *wherein* the receiver is further adapted to create (131) an impedance mismatch (reflection)

to indicate that the second core is unable to transfer the data, and wherein the transmitter is adapted to detect the impedance mismatch (the reflection) ".

In response, Applicants respectfully contend that Lindsey does not teach that a semiconductor device that comprises a transmission line that electrically connects an **output** of a line **driver** to an **input** of a line **receiver** as taught by Applicant's Claims 1 and 11. In contrast, Lindsey teaches in FIG. 1 and col. 2, lines 50 and 56, a transmission line (i.e., a combination of trace 104, 130, and 124) connected to an " **input** of **receiver** 105" **and** an " **input** of **receiver** 125. Applicants argue that Lindsey teaches two **receivers** connected at their **inputs**. Therefore, Applicants contend that Lindsey does not teach a transmission line that electrically connects an **output** of a line **driver** to an **input** of a line receiver as taught by Applicant's Claims 1 and 11.

Third example

As a third example, Applicants respectfully contend that Lindsay does not teach the feature of "wherein the receiver is further adapted to create an impedance mismatch to **indicate** that the **second core** is **busy** performing functions and is **unable to transfer the data**" (emphasis added).

The Examiner alleges that "Lindsey et al. teaches all claimed features in Fig. 1...wherein the receiver is further adapted to create (131) an impedance mismatch (reflection) to indicate that the second core is unable to transfer the data"

In response, Applicants respectfully contend that Lindsey does not teach that a semiconductor device that creates an impedance mismatch to **indicate** that a second core is **busy** performing functions and is **unable to transfer data** between a first core and a second core as

taught by Applicant's Claims 1 and 11. In contrast, Lindsey teaches in FIG. 1 and col. 3, lines 18-33, an impedance discontinuity to generate an early reflection back to chip 11 to allow a first zero bit from chip 12 to be correctly recognized. Therefore, Applicants contend that Lindsey does not teach an impedance mismatch to **indicate** that a second core is **busy** performing functions and is **unable to transfer data** as taught by Applicant's Claims 1 and 11.

Based on the preceding arguments, Applicants respectfully maintain that Lindsay does not anticipate claims 1 and 11, and that claims 1 and 11 are in condition for allowance. Since claims 2-4 and 6 depend from claim 1 and claims 12-15 and 19 depend from claim 11, Applicants contend that claims 2-4, 6, 12-15 and 19 are likewise in condition for allowance.

35 U.S.C. § 103(a)

The Examiner rejected claims 5 and 20 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lindsay *et al.*

In response, Applicants contend that since claim 5 depends from claim 1 and claim 20 depends from claim 11 which Applicants have argued *supra* to not be unpatentable over Lindsey under 35 U.S.C. §102(e), Applicants maintain that claims 5 and 20 are likewise not unpatentable over Lindsey under 35 U.S.C. §103(a).

The Examiner rejected claims 7-10 and 16-18 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lindsay *et al.* In view of Martin *et al.* (U.S. Pat. 6,639,423).

In response, Applicants contend that since claims 7-10 depend from claim 1 and claims 16-18 depend from claim 11 which Applicants have argued supra to not be unpatentable over Lindsey under 35 U.S.C. §102(e), Applicants maintain that claims 7-10 and 16-18 are likewise not unpatentable over Lindsey in view of Martin under 35 U.S.C. §103(a).

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0457.

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Mark J. Friedman
Registration No. 57,918

Schmeiser, Olsen & Watts
3 Lear Jet Lane, Suite 201
Latham, New York 12110
(518) 220-1850